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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/602,488 | 06/23/2003 | Tatyana N. Andryushchenko | 42P16161 | 1128 |

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| EXAMINER | |
|---|---|
| GURLEY, LYNNE ANN | |
| ART UNIT | PAPER NUMBER |
| 2812 | |

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/602,488 | ANDRYUSHCHENKO ET AL. | |
| | Examiner | Art Unit | |
| | Lynne A. Gurley | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22 and 34-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 34-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the remarks filed 12/13/04.

Currently, claims 1-22 and 34-44 are pending.

### *Specification*

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 103*

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-22 and 34-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uzoh et al. (US 6,780,772, dated 8/24/04, filed 12/21/01) in view of Berman et al. (US 6,739,953, dated 5/25/04, filed 4/9/03).

Uzoh shows the method substantially as claimed, in figures 1-9 and corresponding text, as providing a wafer 202 (fig. 4), the wafer comprising an inter-layer dielectric (ILD) 210 having a feature therein 204 (fig 4; column 4, lines 50-61), an underlayer 208 (the first layer of the multi-layered barrier layer; column 4, lines 61-67) deposited on the ILD, a barrier layer 208 (remaining layers of the multi-layered barrier layer) deposited on the under-layer and a conductive layer 206 (Cu; column 5, lines 1-4) deposited on the barrier layer; exposing the barrier layer (Fig. 9A) and removing the barrier layer (fig. 9B). The removal of the barrier layer and the conductive layer is performed by electropolishing (column 8, lines 37-67; column 9, lines 1-7). The conductive layer is copper. The barrier comprises tantalum (Ta). The under-layer is TaN. A portion of the under-layer and/ or the conductive layer may be removed using CMP (column 8, lines 37-67; column 9, lines 1-7).

Uzoh lacks anticipation only in not explicitly teaching the specifics of the electropolishing process, i.e.: 1) that the wafer is placed in an electrolyte, such that at least the barrier layer is immersed in the electrolyte; and an electrical potential is applied between the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed; 2) the electrolyte has a pH equal to or greater than 10; 3) the electrolyte comprises a solution of KOH, NaOH, NH4OH or TMAH; 4) an additive is added to the electrolyte; 5) the

additive is an oxidizer, a corrosion inhibitor, a surfactant, a buffer, a complexor or combinations thereof; and 6) the electric potential has a value equal to or greater than 0.5V with respect to the saturated calomel reference electrode.

Berman teaches an electropolishing apparatus used to remove conductive layers from a substrate with an electrolytic slurry and an applied voltage. The definition and mechanics of electropolishing are taught (column 4, lines 41-60; also, see column 2, lines 24-57; column 5, lines 39-57; column 6, lines 8-45 – teaches removal of the barrier layer; column 7, lines 63-67; column 8, lines 1-20). Additives to the electrolyte are discussed in order to keep the electrolyte the proper consistency (column 7, lines 8-30).

It would have been obvious to one of ordinary skill in the art to have placed the wafer in an electrolyte, such that at least the barrier layer is immersed in the electrolyte; and to have applied an electrical potential between the wafer and an electrode immersed in the electrolyte until at least part of the barrier layer is removed, in the method of Uzoh, as taught by Berman, with the motivation that Uzoh uses an electropolishing method to remove the barrier and the conductive layers, while Berman teaches the electropolishing apparatus for the same purpose and, additionally, gives the definition of the electropolishing process, including the immersion of the conductive layers in the electrolyte and the applied electrical potential between the wafer and an electrode immersed in the electrolyte in order to remove of the conductive layers.

It would have been obvious to one of ordinary skill in the art to have had the electrolyte have a pH equal to or greater than 10; to have had the electrolyte comprise a solution of KOH, NaOH, NH4OH or TMAH; to have added an additive to the electrolyte; to have had the additive be an oxidizer, a corrosion inhibitor, a surfactant, a buffer, a complexor or combinations thereof;

and to have had the electric potential have a value equal to or greater than 0.5V with respect to the saturated calomel reference electrode, in the method of Uzoh, as supported by Berman, with the motivation that these are all conventional additives which adjust the rate and efficiency of removal in a conductor removal process (i.e. CMP), especially in the absence of any showing of criticality and, with the motivation that Berman teaches the modification of the electrolyte by various means to keep a desired consistency to optimize the process and adapt the process to different conductive layers (column 7, lines 8-30). Additionally, the electropolishing process may be optimized to control any varying local electric fields by changing the voltage applied, the additives which can act as plating suppressors or antisuppressors to modulate the electropolishing (See Cox, US 6,383,917 cited in the PTO Form 892; column 4, lines 48-60).

***Response to Arguments***

5. Applicant's arguments filed 12/13/04 have been fully considered but they are not persuasive. In response to Applicant's remarks, page7, regarding Uzoh and Berman both disclosing "wafers including a barrier layer deposited directly on the dielectric layer and a sees metal layer deposited on the barrier layer", Uzoh discloses a multi-layered barrier layer (column 4, lines 61-67, which when broadly interpreted, means that since Uzoh discloses more than one layer for the barrier layer, one of the layers may also function as Applicant's broad limitation of an "under-layer". Therefore, clearly, the under-layer and the barrier are disclosed in Uzoh. Berman is cited for the details of the electropolishing process. Berman continues with Uzoh's process after the barrier layer, to give details of the electropolishing process.

6. Additionally, in response to Applicant's remarks, page 8, using the broadest interpretation of the claim, and considering the open "comprising" language Applicant uses, the use of a slurry is not precluded from Applicant's claims. The electrolyte is combined with the slurry. Again, see column 4, lines 41-60 and also, see lines 60-67; column 5, lines 1-67, wherein the electrolytic solution is dispensed on the polishing pad, etc. Clearly, the broadest interpretation lends itself to the fact that the wafer surface is in the electrolyte solution.

Finally, the above response is applicable to the remarks on pages 8-9.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lynne A. Gurley

Primary Patent Examiner

TC 2800, Art Unit 2812

LAG

March 20, 2005